TRANSMITTAL MESSAGE COVER SHEET

DATE: September 4, 2002

Please deliver the following pages to:

NAME: **Examiner Ron Pompey**
Group 2812
FAX NO.: (703) 746-3919
PHONE NO.:

FROM:
NAME: Gregory E. Montone, Esquire
Antonelli, Terry, Stout & Kraus
FAX NO.: (703) 312-6666
PHONE NO.: (703) 312-6600

MESSAGE:

Re: U.S. Serial No. 09/416,959

Dear Examiner Pompey:

Enclosed please find a copy of the Amendment which we filed on September 3, 2002 regarding the above matter. I will look forward to discussing this amendment with you during our interview tomorrow afternoon.

TOTAL NUMBER OF PAGES INCLUDING COVER SHEET: 12

501.35437CV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YOSHIDA et al.

Serial No.: 09/416,959

Filed: October 13, 1999

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR MANUFACTURING THE SAME

Group: 2812

Examiner: R. Pompey

AMENDMENT

Assistant Commissioner
for Patents
Washington, D.C. 20231

September 3, 2002

Sir:

In response to the Office Action dated April 2, 2002, the period of response for which extension is requested by the attached Petition for Extension of Time, please amend the above-identified application as follows:

In the Claims:

Please cancel claims 18-41 without prejudice.

Please add new claims 42-49 as follows:

– 42. A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;